1. A differential sampling circuit employing a switched-capacitor approach for generating a real differential input signal DC offset value at each period of a system clock, the circuit having first and second input signals (Vin+,Vin-) input thereto, the circuit comprising:

a differential operational amplifier having a positive input and a negative input, the positive output generating a first output signal Vout+ and the negative output generating a second output signal Vout- defining a differential output signal ΔVout therebetween;

a first switched-capacitor network including

a first capacitor coupled to said positive input and to a first node,

a first switch coupled to said first node and to a first terminal supplying the first input signal (Vin+),

a second switch coupled to said first node and to ground,

a third switch coupled to said positive input and to said negative output,

a fourth switch coupled to said negative output and to a second node,

a fifth switch coupled to said second node and to ground;

a second capacitor coupled to said positive input and to the second node,

a sixth switch coupled to said first node and to the negative output,

a third capacitor coupled to said positive input and to a third node,

a seventh switch coupled to said third node and to ground, and

an eighth switch coupled to said first node and to said third node;

a second switched-capacitor network including

a fourth capacitor coupled to said negative input and to a fourth node,

a ninth switch coupled to said fourth node and to a second terminal supplying the second input signal (Vin-),

a tenth switch coupled to said fourth node and to ground,

an eleventh switch coupled to said negative input and to said positive output,

a twelfth switch coupled to said positive output and to a fifth node,

a thirteenth switch coupled to said fifth node and to ground,

a fifth capacitor coupled to said negative input and to the fifth node,

a fourteenth switch coupled to said fourth node and to said positive output,
a sixth capacitor coupled to said third negative input and to a sixth node,
a fifteenth switch coupled to said sixth node and to ground, and
a sixteenth switch coupled to said fourth node and to said sixth node;

wherein

said first capacitor and said third capacitor have equal values,
said fourth capacitor and said sixth capacitor have equal values, and
said switches are selectively set in response to control signals in either an open or a closed state according to a determined algorithm within one period of said system clock.

2. The sampling circuit of claim 1 wherein said control signals are generated by timing control means receiving the system clock.

3. The sampling circuit of claim 1 wherein the first, ninth, third, eleventh, fifth, and thirteenth switches are closed while the second, tenth, fourth, twelfth, sixth, fourteenth, seventh, fifteenth, eighth and sixteenth switches are open during at least a first portion of the first half period.

4. The sampling circuit of claim 1 wherein the second, tenth, fourth, and twelfth switches are closed while the first, ninth, third, eleventh, fifth, thirteenth, sixth, fourteenth, seventh, fifteenth, eighth and sixteenth switches are open during at least a second portion of the first half period.

5. The sampling circuit of claim 1 wherein the first, ninth, third, eleventh, seventh, and fifteenth switches are closed while the second, tenth, fourth, twelfth, fifth, thirteenth, sixth, fourteenth, eighth and sixteenth switches are open during at least a first portion of the second half period.

6. The sampling circuit of claim 1 wherein the fifth, thirteenth, sixth, fourteenth, eighth, and sixteenth switches are closed while the first, ninth, second, tenth, third, eleventh, fourth, twelfth, seventh and fifteenth switches are open during at least a second portion of the second half period.

7. A differential sampling circuit for generating a real differential input signal DC offset value at each period of a system clock, the circuit comprising:

a differential operational amplifier having an input terminal and an output terminal, and characterized by a DC offset voltage;

a first capacitor and a second capacitor each having a first terminal and a second terminal, each said first terminal being connected to the input terminal, said first capacitor and said second capacitor being matched with respect to capacitance value;

wherein

the charge on the first capacitor is proportional to the DC offset voltage during an input signal sampling operation in a portion of each system clock period, and

the first capacitor and the second capacitor are connected in parallel during a charge transfer operation in a subsequent portion of each system clock period.

8. A differential sampling circuit according to claim 7, wherein

an output terminal voltage during said charge transfer operation is proportional to a sum of a first input voltage applied to the input terminal during a first signal sampling operation and a second input voltage applied to the input terminal during a second signal sampling operation in another portion of the system clock period, said output terminal voltage being independent of the DC offset voltage.

9. A differential sampling circuit according to claim 8, wherein each period of the system clock comprises a first half period and a second half period, the first input signal sampling operation is during the first half period, the second input signal sampling operation is during the second half period, and the charge transfer operation is subsequent to the second input signal sampling operation during the second half period.

10. A differential sampling circuit according to claim 7, further comprising a plurality of switches so that said first capacitor, said second capacitor and said switches form a switched-capacitor network, and wherein said switches are selectively set in response to control signals in either an open or a closed state according to a determined algorithm within one period of the system clock.